**1.Question 1**

Which are reasonable approaches for designing a fast, scalable, programmable data plane?

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**Make software routers faster by distributing software routers across clusters.**

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**Make software routers faster by reducing the need to copy packets from the kernel into user space.**

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**Make hardware routers more programmable with custom OpenFlow chips.**

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**Make software routers faster by amortizing packet-processing costs across batches of packets.**



Send all traffic through software switches running in user space

1 point

**2.Question 2**

What are functions that are commonly performed by a programmable data plane?



Specifying access control policies



Learning the mappings between output ports and source addresses



**Forwarding**

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**Maintaining statistics about traffic (e.g., traffic counters)**

****

**Enforcing access control decisions**

**3.Question 3**

Which of the following functions might be performed by a Click element?



**Dropping packets**



Computing shortest paths routes between two routers



**Reading a packet from a network device**

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**Classifying packets into different priority queues**

****

**Counting packets**

**4.Question 4**

Which of the following are true about programmable data planes in Click?



**Click elements can be composed to perform complex functions, such as the forwarding at an IP router.**



Data-plane processing in Click is limited to a fixed set of elements provided by the software.



Click configuration is a simplified version of Python.



Click elements can be composed to perform complex network-wide functions, such as shortest paths or BGP routing.



Click elements cannot perform common data plane operations such as TTL decrement or checksum computations.

**5.Question 5**

Suppose a RouteBricks routers with one intermediate switching stage and 5 servers, each with five 1 Gbps ports. What is the required per-server processing rate, assuming that traffic is not necessarily uniform?



1 point

**6.Question 6**

Why does a RouteBricks server assign one core per queue?



Having multiple cores accessing the same queue would require each core to perform only one function in the packet processing pipeline, which is inefficient.



**Having multiple cores accessing the same queue would require locking to prevent concurrent memory accesses, slowing packet forwarding performance.**



Cores have heterogeneous performance, and packets are different sizes, so it makes sense to assign less powerful cores to queues that have smaller packets.



Having multiple cores accessing the same queue might create the possibility that there is a queue that is not served by any cores.

1 point

**7.Question 7**

What are some tricks commonly employed in software to accelerate packet forwarding?



Forwarding smaller packets before larger packets



**Avoiding lookups on the software bridge between virtual interfaces and physical interfaces**

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**Batch processing**

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**Large packet buffers that hold multiple packets that can be read with a single read**

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**Ethernet GRE tunnels**

1 point

**8.Question 8**

What are some of the problems with current OpenFlow hardware that motivated a custom OpenFlow chip design?



**Current hardware makes it difficult to implement multiple match action stages, and to repurpose TCAM and SRAM across multiple match-action stages.**

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**The current OpenFlow protocol depends on the constraints of conventional switching chips.**



Current hardware cannot support OpenFlow 1.0 match-action primitives.



**Current hardware is difficult to repurpose in the field.**



Current hardware cannot forward traffic at line rates.

1 point

**9.Question 9**

Which of the following are motivations for SwitchBlade, which supports composition of pre-synthesized hardware data plane modules on an FPGA?



Programming in C is difficult.



FPGAs are lower-cost and consume less power than conventional ASICs or OpenFlow switching chips.



**Programming in Verilog is difficult.**

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**Most data plane protocols involve composing only a limited number of data-plane actions.**

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**Experimental data planes may need to operate in parallel with production data planes.**

1 point

**10.Question 10**

Which of the following are true about the current OpenFlow chip design described in the lesson?



**Actions can be applied to different header fields in parallel.**



The OpenFlow chip requires about twice as much chip area as a conventional switching chip.



The OpenFlow chip can perform arbitrary packet processing operations, such as deep packet inspection.



**Memory can be mapped arbitrarily across different stages of the match-action pipeline.**

****

**The architecture is based on a reduced instruction set, so that as chips become faster, packet forwarding speeds should also increase.**

1 point